(3)

PROGRAMMABLE RESOLUTION CMOS IMAGE SENSOR

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to U.S. Provisional Patent Application, Serial No. 60/252,892, filed November 27, 2000, which is incorporated in its entirety by reference herein.

FIELD OF THE INVENTION

The present invention relates to image sensors generally and to programmable resolution image sensors in particular.

BACKGROUND OF THE INVENTION

Image processing of various types involves trading image resolution against other desired characteristics. For example, image recognition processing speed is highly dependent on the number of processed pixels per frame and therefore, the higher the desired speed, the lower the resolution should be. Similarly, tracking of fast moving objects might dictate frame rates higher than those acceptable to the human eye, such as 30 frames/sec (NTSC) or 25 frames/sec (PAL).

A simple technique to accomplish higher frame rates is called "pixel dilution" and it involves skipping over and reading out every n-th pixel in a row, and every m-th row. This results in a higher frame rate, but also in a lower resolution.

More sophisticated methods may involve image processing. In the prior art, the image processing was done away from the focal plane. Recently, with the revival of active pixel sensor (APS) -based CMOS image sensors, there is a tendency to embed image processing functions on the same die with the image sensor, as close as possible to the focal plane or in the focal plane itself.

Much of the work on varying the image sensor's resolution has been performed in the last decade, in context with the APS-photo-gate type image sensors. An image sensor, which is configurable to yield varying resolution images, is a multiresolution image sensor. Such a sensor

has row and column averagers, which combine a configurable number of same-row adjacent pixels, and a configurable number of adjacent columns, and output a row/column block average. These averagers are implemented just ahead of the image sensor's video output and follow the data acquisition from the focal plane. The method outputs less "pixels" and therefore allows for higher frame rates. It also "smoothes" the image. The method is less than optimal and has several disadvantages, as follows:

• The averaging is performed in proximity to, but not on the focal plane. Provided that focal plane averaging is feasible, there is some Signal to Noise Ratio (SNR) loss involved. Averaging circuitry also produces some SNR loss. SNR loss is not desirable especially for low lighting conditions, where acquisition of a decipherable image is difficult.

• The averaging circuits add complexity to the image sensor.

Frame Transfer Image Sensors are also known, which performs the multiresolution function outside of the analog memory array itself. This type of sensor utilizes the fact that the stored charges of adjacent analog memory add "naturally". Adding the charges rather than averaging them results in an improved SNR, which is very important for weak signals in bad lighting conditions. The disadvantage of this method lies once again in the fact that the charge addition is performed off the focal plane after some loss in the signal strength, and some noise has been added.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a novel image sensor.

In accordance with a preferred embodiment of the present invention, an image sensor is described which trades resolution for improved SNR and for higher frame rates. The charge or current from a unit cell adds naturally and therefore allows signals to be combined at the focal plane.

Furthermore, the present invention provides an image sensor which can operate in a non-interlace, as well as in an interlace mode. The method allows for an improved SNR at little or no resolution degradation, when the sensor operates in interlace mode.

There is therefore provided, in accordance with a preferred embodiment of the present invention, an image sensor which includes a plurality of unit cells, each adapted to generate charge in response to photons incident thereon and array elements adapted to sum charge from one or more unit cells at a focal plane of the image sensor.

There is also provided, in accordance with a second preferred embodiment of the present invention, an image sensor which includes a plurality of unit cells, each adapted to generate charge in response to photons incident thereon and array elements adapted to change a resolution of the output of the image sensor at its focal plane.

Additionally, in accordance with a preferred embodiment of the present invention, the array elements include charge transfer transistors, one per unit cell, a line decoder and a column selector. The charge transfer transistors are adapted to transfer charge from their associated unit cells when activated. The line decoder is adapted to activate charge transfer transistors of one or more lines of unit cells and the column selector is adapted to activate one or more columns of unit cells and to combine the charge transferred by activated charge transfer transistors of the activated columns.

Moreover, in accordance with a preferred embodiment of the present invention, the array

elements include an adjacent line unit adapted to indicate to the line decoder to activate at least two adjacent lines and to the column selector to select one column thereby to combine charge from the corresponding unit cells in adjacent lines.

Furthermore, in accordance with a preferred embodiment of the present invention, the array elements include an adjacent column unit adapted to indicate to the line decoder to activate one line and to the column selector to combine charge of at least two columns thereby to combine charge from at least two unit cells in adjacent columns.

Further, in accordance with a preferred embodiment of the present invention, the array elements include a block unit adapted to indicate to the line decoder to activate U adjacent lines and to the column selector to combine charge of V columns thereby to combine charge from UxV unit cells in a UxV block.

Still further, in accordance with a preferred embodiment of the present invention, the image sensor also includes an interlace unit adapted to produce video output from the image sensor in an interlace mode. The interlace unit includes a unit adapted to activate the adjacent line unit to combine charge of pairs of unit cells in adjacent lines beginning with the odd lines for an odd field output and of adjacent lines beginning with the even lines for an even field output.

Moreover, in accordance with a preferred embodiment of the present invention, the image sensor also includes an intercolumn unit adapted to produce video output from the image sensor in an intercolumn mode. The intercolumn unit includes a unit adapted to activate the adjacent column unit to combine charge of pairs of adjacent columns beginning with the odd columns for an odd field output and of adjacent columns beginning with the even columns for an even field output.

Further, in accordance with a preferred embodiment of the present invention, the image sensor includes a block interlace unit adapted to produce video output from the image sensor in a block interlace mode. The block interlace unit includes a unit adapted to activate the block unit to combine charge of 2x2 blocks wherein the blocks of an odd field output begin with the block whose

upper left-hand unit cell is in the first column, first line and wherein the blocks of an even field output begin with the block whose upper left-hand unit cell is in the second column, second line.

Finally, the present invention includes the methods performed by the image sensor.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the appended drawings in which:

Fig. 1 is a circuit diagram illustration of a portion of an image sensor, constructed and operative in accordance with a preferred embodiment of the present invention, showing two unit cells from two adjacent lines and elements for sensing their charge;

Fig. 2 is a circuit diagram illustration of a portion of an image sensor, constructed and operative in accordance with a preferred embodiment of the present invention, showing two unit cells from two adjacent columns and elements for sensing their charge;

Fig. 3 is a block diagram illustration of one embodiment of the image sensor of the present invention;

Figs. 4A, 4B and 4C are schematic illustrations of three modes of generating programmable resolution;

Figs. 5A, 5B and 5C are schematic illustrations of three modes of achieving interlace signals using the image sensor of the present invention;

Fig. 6 is a block diagram illustration of a further embodiment of the image sensor of the present invention;

Fig. 7 is a block diagram illustration of a line decoder forming part of the image sensor of Fig. 6;

Fig. 8 is a block diagram illustration of a column selector decoder forming part of the image sensor of Fig. 6; and

Fig. 9 is a block diagram illustration of a video multiplexer forming part of the image sensor of Fig. 6.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

Reference is now made to Fig. 1 and 2, which illustrate two alternative embodiments of the present invention. Both figures show two adjacent unit cells, where the two unit cells in Fig. 1 are in the same column and the two unit cells of Fig. 2 are in the same row. Both unit cells are of the direct injection, charge-sensing type.

In the present invention, the charge of adjacent cells may be separately sensed or may be combined, as desired. When the charge is separately read, the resolution is high (i.e. there are more pixels). When the charges are combined, the resolution is lower (i.e. fewer pixels); however, the signal to noise ratio (SNR) is much higher in this latter case than for the higher resolution case.

As can be seen in Figs. 1 and 2, described in more detail hereinbelow, the programmable resolution function is combined with the sense function, at the output of the unit cells. Therefore, the noise contribution to the video signal is minimal. Furthermore, the present invention improves the signal to noise ratio since it simply adds the charge or current of adjacent unit cells rather than averaging the charge or current.

Figs. 1 and 2 depict two "adjacent" unit cells UC_1 and UC_2. These unit cells are Direct Injection (DI) - Charge-Sensing Unit Cells. "Adjacent" is defined as being located near each other in the array and meeting the following conditions:

Let Q_1 and Q_2 be the charge signals accumulated in adjacent unit cells, UC_1 and UC_2, respectively. Then

$$(1)\ Q_1 = \overline{Q} + \varepsilon$$

$$(2)\ Q_2 = \overline{Q} - \varepsilon$$

where,

$$(3)\ \overline{Q} = \frac{Q_1 + Q_2}{2}$$

and,

$$(4)\ \varepsilon = \frac{Q_1 - Q_2}{2}$$

$$(5)\ \left|\frac{\varepsilon}{Q}\right| << 1$$

Same Column/Adjacent Rows

Fig. 1 depicts two adjacent unit cells UC_1 and UC_2 located in the same column and in two adjacent rows. Each cell comprises a photodetector PD_i, a charge integration control unit 10, a charge integration capacitor CI_i and a charge readout transistor TR_i. Transistors TR_i are controlled by line read signals $LnRd_i$ and the array includes a sense amplifier SA per every two unit cells UC, connected to the output of the transistors TR_i via a column line 12.

Each photodetector PD is light sensitive and produces a photocurrent proportional to the intensity of light. Each control circuit 10 controls the photocurrent charge integration period (or exposure time) over each integration capacitor CI. Following the image acquisition, which occurs during exposure, the charge stored in each integration capacitor CI is proportional to the photocurrent and length of exposure. The charge stored in each integration capacitor CI is then read out. A transition on the relevant LnRd signal from "0" to "1" causes the relevant readout transistor TR to turn ON, which results in readout of the stored charge. In other words, the charge stored on the relevant integration capacitor CI is transferred via column line 12 to sense amplifier SA.

It will be appreciated that the present invention incorporates any operation that causes a readout transistor to be turned on. This can be a transition to "1" for an n-channel type transistor or a transition to "0" for a p-channel type transistor.

Sense amplifier SA is a charge integration amplifier and comprises an amplifier A, a charge integration capacitor C and a switch S that resets the capacitor C (e.g. reduces the capacitor's charge to zero). To achieve the highest resolution, the charges Q_1 and Q_2 are readout separately.

For instance, providing a transition on $LnRd_1$ signal causes readout transistor TR_1 of unit cell UC_1 to transfer charge Q_1 from integration capacitor CI_1 to sense amplifier SA. At the end of charge transfer process, charge Q_1, resides on capacitor C. Accordingly, the output voltage V_{out1} of sense amplifier SA is, for unit cell UC_1:

$$(6)\ |V_{out1}| = \frac{1}{C} \bullet |Q_1|$$

If the RMS voltage noise signal is e_{n1}, then the signal to noise ratio of the output of sense amplifier S is, for unit cell UC_1:

$$(7)\ SNR_1 = \frac{|V_{out1}|}{e_{n1}}$$

Similarly, if there is a transition on line read signal $LnRd_2$ of unit cell UC_2, the output voltage V_{out2} is:

$$(8)\ |V_{out2}| = \frac{1}{C} \bullet |Q_2|$$

and,

$$(9)\ SNR_2 = \frac{|V_{out2}|}{e_{n2}}$$

where e_{n2} is the RMS voltage noise for charge Q_2 and SNR_2 is the corresponding signal to noise ratio.

For adjacent pixels,

$$(10)\ |V_{out2}| \cong |V_{out1}| = |\overline{V}_{out}| = \frac{1}{C} \bullet |\overline{Q}|$$

and,

$$(11)\ e_{n1} \cong e_{n2} \cong e_n$$

$$(12)\ SNR_1 \cong SNR_2 \cong SNR$$

Higher frame rates can be accomplished by pairing pixels in the same column, and simultaneously reading out the accumulated charge in two adjacent unit cells. The unit cells UC_1 and UC_2 can be read out at the same time by providing a transition on line read signals $LnRd_1$ and $LnRd_2$ at generally the same time, thus causing transistors TR_1 and TR_2 to turn ON generally simultaneously. The accumulated charges Q_1, and Q_2 are transferred from unit cells UC_1 and UC_2 into the capacitor C of sense amplifier SA. Therefore, the signal voltage V_{out} is,

$$(13)\ V_{out} = \frac{1}{C} \bullet |Q_1 + Q_2| = \frac{2}{C} \bullet |\overline{Q}|$$

In other words, the output signal is twice as large when two adjacent unit cells are read out generally simultaneously in comparison to when each cell is read out separately.

For uncorrelated noise sources en_1 and en_2, the equivalent RMS voltage noise source when simultaneously read is,

$$(14)\ e_n = \sqrt{e_{n1}^2 + e_{n2}^2} = \sqrt{2} \bullet e_n$$

Therefore the signal to noise ratio $SNR_{2,1}$ when two adjacent rows/same column pixels are read out simultaneously is:

$$(15)\ SNR_{2,1} = \sqrt{2} \bullet SNR$$

It will be appreciated that summing the signals accumulated in two adjacent unit cells during a single exposure results in an improvement in the signal to noise ratio by a factor of $\sqrt{(2)}$. This involves a reduction in the vertical resolution and an increase in readout rate by a factor of 2.

Same-Row/Adjacent Columns

Fig. 2 depicts two unit cells UC_3 and UC_4 in the same row but in two adjacent columns,

two sense amplifiers SA_1 and SA_2 and an amplifier selector AS. Each unit cell UC_3 and UC_4 has the same elements as the unit cells of Fig. 1 and will not be described further. Each sense amplifier SA_1 and SA_2 has the same elements as the sense amplifier of Fig. 1 and will not be described further. Amplifier selector AS operates to steer charge from unit cells UC_3 and UC_4 into sense amplifiers SA_1 and SA_2 and comprises four select transistors T_1, T_2, T_3, and T_4 that are controlled by control signals CS_1, CS_2, CS_3 and CS_4, respectively.

Select transistors T_1 and T_4 connect the column lines 1 and 3, respectively, directly to sense amplifiers SA_1 and SA_2, respectively. Select transistors T_2 and T_3 connect column line 2 to either sense amplifier SA_1 or SA_2.

For the highest resolution, the charge from each unit cell UC_i is read by separate sense amplifiers SA_i. Control signals CS_1 and CS_4 are set to activate select transistors T_1 and T_2 and to deactivate select transistors T_3 and T_4. Thus, the charge stored in unit cell UC_3 is read out through transistor TR_3 to column line 1, through select transistor T_1 in amplifier selector AS to sense amplifier SA_1. Similarly, the charge stored in unit cell UC_4 is read through transistor TR_4 to column line 2, through select transistor T_2 to sense amplifier SA_2. The charges Q_3 and Q_4 are read out generally simultaneously by sense amplifiers SA_1 and SA_2.

Faster readout can be accomplished by combining the charge of the two adjacent same-row pixels into a single sense amplifier. For the case depicted in Fig. 2, charges Q_3 and Q_4 are read into sense amplifier SA_1, while sense amplifier SA_2 is not used. This is achieved by pulling providing a transition on the LnRd signal while generally simultaneously turning on select transistors T_1 and T_3. Select transistors T_2 and T_4 stay in the OFF condition. Table 1 lists the valid states for the four select transistors T_1, T_2, T_3 and T_4.

Table 1:

Select Signal Combination				Connection		
CS_1	CS_2	CS_3	CS_4	In1	In2	In3
"0"	"0"	"0"	"0"	None	None	None
"1"	"1"	"0"	"0"	O_1	O_2	None
"1"	"0"	"1"	"0"	O_1	O_1	None
"0"	"1"	"0"	"1"	None	O_2	O_2

It will be appreciated that when the charge of two adjacent unit cells of the same row are combined, the resolution of the resultant image is half of that if no charge is combined. Furthermore, only generally half of the sense amplifiers contain row information. Therefore, the line readout time is twice as fast. This will also result in halving the entire frame readout time.

A similar SNR analysis to the one performed for the embodiment of Fig. 1 yields a similar result-,

$$(16)\ SNR_{3,4} = \sqrt{2} \bullet SNR$$

where $SNR_{3,4}$ is the signal to noise ratio when the charge of two adjacent same-row unit cells UC_3 and UC_4 are combined into a single sense amplifier while SNR is the signal to noise ratio when charge of one unit cell is read out into an individual sense amplifier.

A block of U-Rows/V-Columns

Reference is now made to Fig. 3, which is a general schematic of an image sensor 20, constructed and operative in accordance with a preferred embodiment of the present invention. Image sensor 20 comprises a multiplicity of unit cells 22, such as the ones described hereinabove with respect to Figs. 1 and 2, a line decoder 24, a column selector 26 and a video output multiplexer (MUX) 28.

Line decoder 24 is capable of selecting, generally simultaneously, a group of U rows where U is a programmable number. Thus, in the first readout cycle, line read signals $LnRd_1$ to $LnRd_u$ have transitions thereon while the remaining lines do not. During the next readout cycle, line read signals $LnRd_{u+1}$, to $LnRd_{2u}$ have transitions thereon while the remaining lines do not, and so

on.

Column selector 26 is capable of selecting, generally simultaneously, a group of V columns where V is a programmable number. Thus, the first V Unit Cells UC_1 to UC_v are generally simultaneously read out to the first sense amplifier SA_1, the second V Unit Cells UC_{v+1}, to UC_{2v} are simultaneously read out to sense amplifier SA_{v+1}, and so on.

Video output MUX 28 outputs the signal from a single sense amplifier to the video output. MUX 28 is programmed to produce the outputs of those sense amplifiers that contain valid information, that is, SA_1, SA_{v+1},SA_{2v+1} and SA_{NV+1}.

Image sensor 20 operates by reading UxV blocks at a time to a single sense amplifier (i.e. the charge of the unit cells in the block are combined and are read by the sense amplifier for the block). U and V are programmable numbers, which control the operation of line decoder 24, column selector 26 and video MUX 28.

For the sake of simplicity, assume that M is divisible by U, and N is divisible by V. We define the following variables:

T_{Pclk} is the basic unit cell clock period, used for readout. Thus readout from a single sense amplifier is performed in a single unit cell clock period.

T^0_{Rd} is the readout time for the entire array for the highest resolution case (i.e. each unit cell is individually read into a separate sense amplifier). For this case:

$$(17)\ T_{Rd}^{O} = M \bullet N \bullet T_{PClk}$$

$T^{U,V}_{Rd}$ is the readout time for a UxV block into a single sense amplifier.

$$(18)\ T_{Rd}^{U,V} = \frac{M}{U} \bullet \frac{N}{V} \bullet T_{PClk}$$

or,

$$(19)\ T_{Rd}^{U,V} = \frac{T_{Rd}^{O}}{U \bullet V}$$

When the stored information is read in U X V blocks, the readout time is reduced by a factor of U*V, the horizontal resolution is reduced by a factor of V, and the vertical resolution by a factor of U.

The signal to noise ratio can determined for two cases, a variable frame rate and a fixed frame rate. Variable Frame Rate: In some applications, such as the acquisition of images of moving object, a variable frame rate is important. When an object is approaching the camera, its angular speed is higher. Therefore, for fast moving objects, more frames per second is essential. The present invention provides this, without unit cell dilution.

In this case, multi-resolution is applied to increase the frame readout. For this case,

$$(20)\ T = \frac{T_{Rd}^{O}}{U \bullet V} + T_I$$

and,

$$(21)\ FR = \frac{1}{T}$$

where,

T_I - is the charge integration time,

T - is the frame cycle time,

FR - is the frame rate.

Formula (20) indicates that higher frame rates can be traded for lower resolutions. The signal to noise ratio $SNR_{u,v}$ can be also derived,

$$(22)\ SNR_{U,V} = \sqrt{U \bullet V} \bullet SNR$$

where SNR is the signal to noise ratio for the highest resolution.

As can be seen, when the unit cells are readout in UxV blocks, the signal to noise ratio improves by a factor of √(U*V).

Fixed Frame Rate: For still video, poor lighting conditions, or when a compressed picture form is desirable (for the sake of saving picture storage space), one may utilize the multi-resolution of the present method to improve the sensitivity of the SNR. For real-time video either displayed on a TV or on a computer monitor, the frame rate is fixed. For this case, the maximum charge integration time is determined by the frame rate and by the readout time, where $T^0_{I,max}$ is the maximum integration time for the case where each unit cell is individually read.

$$(23)\ T^{O}_{I,\max} = \frac{1}{FR} - T^{O}_{Rd}$$

Reading out the video in UxV blocks reduces the readout time by a factor U*V and therefore allows charge integration time to be increased.

$$(24)\ T^{U,V}_{I,\max} = \frac{1}{FR} - \frac{T^{O}_{Rd}}{U \bullet V}$$

Since the signal to noise ratio improves as a square root of the integration charge time, the improvement of the SNR for the fixed frame rate $SNR^{FFR}_{U,V}$ is governed by

$$(25)\ SNR^{FFR}_{U,V} = \sqrt{\frac{U \bullet V - FR \bullet T^{O}_{Rd}}{1 - FR \bullet T^{O}_{Rd}}} \bullet SNR$$

For example, for an image sensor which operates at a fixed frame rate of 30 frames/sec with a 16 msec readout time at the highest resolution has a reduction in horizontal and vertical resolution by a factor of 2 and an improvement in the signal to noise ration by a factor of 2.6.

Image sensor 20 is capable of programmable resolution. Reference is now made to Figs. 4A, 4B, 4C and 4D, which illustrate its operation for four different cases.

Fig. 4A illustrates the highest horizontal resolution but half the vertical resolution. The

charge from two unit cells 30 and 32 in the same column but in adjacent rows is generally simultaneously transferred into the same sense amplifier. This corresponds to the case of Fig.1. The number of lines to be read is half the maximum number while the number of unit cells per line is maximal. To display a full-size picture on a video display, each line of data must be repeated twice. This is normally done from an external frame buffer and not from the image sensor directly.

Fig. 4B illustrates the highest vertical resolution but half the horizontal resolution. The charge from two unit cells 34 and 36 in the same row but adjacent columns is generally simultaneously read into a single sense amplifier. This corresponds to the case of Fig. 2.

Fig. 4C depicts the case for which the resolution is reduced by a factor of two both horizontally and vertically. Thus, the charge from a 2x2 block 38 is combined into one sense amplifier via two adjacent column lines. This results in significant SNR improvement.

The embodiments of Figs. 4A, 4B and 4C show combining unit cells of two lines and/or two columns. It will be appreciated that the present invention incorporates the embodiments of Figs. 4A, 4B and 4C as well as all other embodiments combining multiple lines and/or multiple columns.

Programmable Resolution, Interlace-Mode Image Sensors

TV displays and often computer monitors operate in an interlace mode. This requires that the frame readout be performed in odd and even field sub-cycles where, during the odd field sub-period, the odd lines are readout, while during the even field sub-period, the even lines are readout. The term "interlaced" indicates that the even lines are located in between the odd lines.

In the present invention, a simple way to generate an interlaced signal is by the acquisition of lines 1, 3, 5. 7, ... for the odd field while reading out the previous even field data and then reading out the odd field data while acquiring the even lines 2, 4, 6, 8, ... for the even field, and so on.

Since each field readout time is half the frame readout time, this results in the reduction of the maximum integration time by a factor of two.

Therefore,

$$(26)\ SNRI = \frac{1}{\sqrt{2}} \bullet SNR$$

where $SNRI_{2,1}$ is the signal to noise ratio for the interlaced image sensor, SNR is the SNR for a conventional sequential, frame-type image sensor programmed to its highest resolution.

Reference is now made to Fig. 5A, which illustrates the operation of the present invention in interlace mode. For the odd field, the charges from two vertically adjacent unit cells 40 and 42 in lines R1 and R2 are combined (as noted by the dashed box around them) and simultaneously transferred to the sense amplifier for that column, SA_1, in a manner similar to that described with respect to Fig. 1. This is true for all unit cells in lines R1 and R2 (i.e. charges from two vertically adjacent unit cells of column C2 are combined and simultaneously transferred to the sense amplifier for that column, SA_2, etc.). This is followed by a similar action for lines R3 and R4, followed by lines R5 and R6, and so on, until the last two lines.

The odd field readout is followed by the readout of the even field. The even field data acquisition is generally simultaneous with the odd field readout. The even field readout involves pairing of lines R2 and R3 (as indicated by the dotted box around the unit cells), followed by lines R4 and R5, followed by lines R6 and R7, and so on.

For this mode of operation the signal to noise ratio $SNRI_{2,1}$ is,

$$(27)\ SNRI_{2,1} = SNR$$

and,

$$(28)\ SNRI_{2,1} = \sqrt{2} \bullet SNRI$$

Reference is now briefly made to Fig. 5B, which illustrates horizontal field interlacing, in a method called intercolumn mode. This is accomplished by combining charge from columns C1 and C2 into sense amplifier SA_1, that of columns C3 and C4 into sense amplifier SA_3, that of columns C5 and C6 into sense amplifier SA_5, etc. and reading out the acquired data during the odd field time period. The even field data readout follows by steering columns C2 and C3 into sense amplifier

SA_2, columns C4 and C5 into sense amplifier SA_4, columns C6 and C7 into SA_6 and reading out the acquired data during the even field time period. This mode yields almost the same resolution as the non-interlaced/highest-resolution mode, since the number of unit cells per line is effectively the same.

The method can be used in the context of non-interlaced displays, if an external video buffer is used to reorder the frame in a way suitable for a display, that is, that the odd "pixel" which combines columns j and j+ 1 will be followed by the same-line adjacent even "pixel" which combines columns j+l, and j+2. While this method does not have any SNR advantages over the standard, non-interlace/highest resolution mode, it does result in further SNR gains, no resolution cost and almost no hardware complications.

Fig. 5C shows a further interlace method where each output "pixel" is formed from a 2x2 block of unit cells. The odd field begins with block 50 having the unit cells from adjacent columns beginning with the odd columns (i.e. columns 1, 3, 5, etc) and adjacent lines beginning with the odd lines (i.e. lines 1, 3, 5). Thus, block 50 has unit cells (R1, C1), (R1, C2), (R2, C1) and (R2, C2). The next block, block 52, has unit cells (R1, C3), (R1, C4), (R2, C3) and (R2, C4). The even field begins with block 54 having the unit cells from adjacent columns beginning with the even columns (i.e. columns 2, 4, 6, etc) and adjacent lines beginning with the even lines (i.e. lines 2, 4, 6). Thus, block 54 has unit cells (R2, C2), (R2, C3), (R3, C2) and (R3, C3). The next block, block 56, has unit cells (R2, C4), (R2, C5), (R3, C4) and (R3, C5).

It is noted that displays are designed to correctly position the even lines between the odd lines. However, there is no mechanism that positions the even columns between the odd columns. Therefore, the image sensor must be designed to account for this. For example, for the even field, and the horizontal interlace mode, the image sensor must delay all the lines by one additional unit cell clock period Tpclk.

It is also noted that the description hereinabove assumes that M and N are even numbers.

Therefore, there is one less row and one less column in the even field compared to the odd field. If N or M are odd, the number of rows or the number of columns, respectively, will be the same for the two fields.

The method of Fig. 5C produces almost the same horizontal and vertical resolution as an image sensor operating in a non-interlace/highest-resolution mode; however, the method of Fig. 5C has a better SNR. The maximum integration time is no different than for the interlaced mode, as described for the case depicted in Fig. 5A. However, the method of Fig. 5C provides a signal with twice the magnitude. This, of course, results in an improved SNR-,

$$(29)\ SNRI_{2,2} = \sqrt{2} \bullet SNR$$

and,

$$(30)\ SNRI_{2,2} = 2 \bullet SNRI$$

where $SNRI_{2,2}$ is the signal to noise ratio for Fig. 5C, in which the charge of four adjacent unit cells are combined into a single sense amplifier.

The present invention has been described for direct injection (DI) type of unit cells, which are based upon charge readout. The present invention also applies to unit cells that are based upon current readout.

The present invention is not limited to summing up the output of two vertically adjacent or two horizontally adjacent unit cells. As described in the context of Fig. 3, any rectangular block of neighboring pixels charges can be added in non-interlace or interlace modes. This reduces the resolution and results in a higher frame rate and an improved SNR, but adds to the hardware complexity.

It will be appreciated that the present invention is unique in that it adds charge right in the focal plane. This results in a lower noise compared to methods for which this is done later in the signal chain. It also results in a stronger signal coming out of the array, and therefore in an improved SNR.

Reference is now made to Figs. 6, 7, 8 and 9, which illustrate various elements necessary to control the image sensor, and its different modes of operation, described hereinabove. Fig. 6 illustrates an image sensor 100, constructed and operative in accordance with a preferred embodiment of the present invention and using the methods described hereinabove with respect to Figs. 1 – 5, Fig. 7 illustrates a line decoder, Fig. 8 illustrates a column selector and Fig. 9 illustrates a video multiplexer. The implementations described hereinbelow are not the only alternatives and all embodiments are incorporated in the present invention.

In accordance with the principles outlined hereinabove, image sensor 100 is fully programmable and can operate in either the interlace or non-interlace mode, and at full or partial resolution, but with significantly improved SNR and readout. Moreover, the programming may be independently performed for the horizontal and the vertical directions.

Image sensor 100 comprises a unit cell array 102, left and right line decoders 104 and 106, respectively, a column selector 108 and a video multiplexer 110. Left and right line decoders 104 and 106 are typically implemented with the same structure, where each decoder has M line read $LnRd_i$ output signals; however, right line decoder 106 is shifted down by one line. Thus, $LnRd_1$ for left line decoder 104 is connected to line 1 of the array while $LnRd_1$ for right line decoder 106 is connected to line 2 of the array, and so on. For right line decoder 106, $LnRd_M$ is not connected to any line. Lines 2 – M of the array are connected to both line decoders 104 and 106 while line 1 is connected to left line decoder 104 only. This arrangement facilitates both the non-interlace and the interlace modes of operation.

For the non-interlace mode, the line readout operation is wholly governed by left line decoder 104.

For the odd field of the interlace mode, the operation is governed by left line decoder 104 and the lines are read out in pairs. Thus, readout of lines 1 and 2 is followed by lines 3 and 4, etc. until lines M-1 and M.

For the even field the operation is governed by right line decoder 106. Right line decoder 106 performs the same operation as for the odd field but the output is shifted due to right line decoder 106 being connected to the array starting at line 2 rather than at line 1 as for left line decoder 104. Thus, readout of lines 2 and 3 is followed by readout of lines 4 and 5, etc. until lines M-2 and M-1.

Fig. 7 details line decoders 104 and 106. This decoder is capable of selecting an individual line or selecting a pair of neighboring lines. The decoder comprises a pre-decoder 111 and a plurality of row selectors (RSel) 112. Pre-decoder 111 determines which line pairs to activate while row selectors activate the selected rows.

Pre-decoder 111 has k address inputs and M/2 outputs, where k is defined as:

$$\log_2 M > k \geq \log_2 M - 1$$

and the output signals are pair line signals $Ln_{1,2}$, $Ln_{2,3}$, etc. Pre-decoder 111 selects a line pair and is implemented as a conventional decoder structure.

The output behavior of pre-decoder 111 is defined as:

Let,

$$(31)\ i = \left(LnAdr_k, LnAdr_{k-1}, LnAdr_{k-2}, \ldots LnAdr_2, LnAdr_1\right)_2$$

where $LnAdr_i$ ="0" or $LnAdr_i$ ="1", $(LnAdr_k LnAdr_{k-1}, LnAdr_{k-2}, \ldots LnAdr_2, LnAdr_1)_2$ is the binary representation of the integer i and

$$1 \leq i \leq \frac{M}{2}$$

With these conditions, the outputs of pre-decoder 110 are either logical "0" or logical "1" subject to the following:

$$(32)\ Ln_{2 \bullet i-1, 2 \bullet i} = En, \text{ and}$$

$$(33)\ Ln_{2 \bullet p-1, 2 \bullet p} = \text{"0"} \text{ for } p \neq i$$

Thus, if En=0, all of the outputs of line decoder 104 or 106 are logical "0". In other words,

setting En to "0" disables the line read operation. This is the default state of line decoders 104/106, when there is no active readout.

The input I of each row selector 112 is connected to one of the outputs $Ln_{2p-1,2p}$ of pre-decoder 111. Each row selector 112 has two outputs O_1 and O_2, which are connected to lines $LnRd_{2p-1}$ and $LnRd_{2p}$, respectively, of array 102 (Fig. 6).

The output signals O_1 and O_2 are functions of input control signals RS_1 and RS_2 and on the input I, driven by the signal $Ln_{2j-1,2j}$, as defined by Table 2:

Table 2:

Inputs			Outputs	
I	**RS_1**	**RS_2**	**O_1**	**O_2**
"0"	"0"	"0"	Z	Z
"1"	"0"	"0"	Z	Z
"0"	"0"	"1"	"0"	"0"
"1"	"0"	"1"	"0"	"1"
"0"	"1"	"0"	"0"	"0"
"1"	"1"	"0"	"1"	"0"
"0"	"1"	"1"	"0"	"0"
"1"	"1"	"1"	"1"	"1"

Where Z is a high-impedance state also called a tristate.

As can be seen from Table 2, the outputs of a row selector 112 are tristated when control signals RS_1="0" and RS_2="0". The tri-state is used most often for the interlace modes of operation

The combinations in Table 2 can be also described by the following formulas:

$$(34)\quad \begin{matrix} O_1 = Z \\ O_2 = "Z \end{matrix} \quad \text{for } RS_1 = "0" \text{ and } RS_2 = "0", \text{ otherwise,}$$

$$(35)\quad \begin{matrix} O_1 = RS_1 \bullet I \\ O_2 = RS_2 \bullet I \end{matrix}$$

The line decoder output lines values are subject to the following-

$$(36)\quad \begin{matrix} LnRd_{2\bullet p-1} = Z \\ LnRd_{2\bullet p} = Z \end{matrix} \quad \text{for } RS_1 = "0" \text{ and } RS_2 = "0", \text{ otherwise,}$$

(37) $LnRd_{2\bullet p-1}$ ="0" and $LnRd_{2\bullet p}$ ="0" for any $p \neq i$ and

$$\begin{aligned} LnRd_{2\bullet p-1} &= RSel_1 \bullet En \\ LnRd_{2\bullet p} &= RSel_2 \bullet En \end{aligned} \quad \text{for } p = i$$

where the function for i is given in (31).

Based upon the values of $Rsel_1$ and $RSel_2$, line decoders 104 and 106 select either a single line or two lines at a time.

For the highest vertical resolution, when each line is individually read, the line signals $LnAdr_1$ to $LnAdr_k$ become active in order, but stay active for a period of two lines. When the odd line is read, $RSel_1$="1" and $RSel_2$="0". When the even line is read, $RSel_1$="0" and $RSel_2$="1".

When programmed for half the vertical resolution, as described in context with Figs. 4A and 4C, two lines are read simultaneously and the line signals $LnAdr_1$ to $LnAdr_k$ become active in order. During the entire readout, $RSel_1$="1"and $RSel_2$="1".

Fig. 8 illustrates programmable column selector 108, which comprises a plurality N/2 of amplifier selectors $AS_{2p-1,p}$ (detailed in Fig. 2), where p is between 1 and N/2, with their inputs connected to the column lines Col_{2p-1}, Col_{2p} and Col_{2p+1} and their outputs connected to the inputs In_{2p-1} and In_{2p} of sense amplifiers SA_{2p-1} and SA_{2p}, respectively. Table 1 hereinabove provides the configurations of amplifier selector AS as functions of the column select signals CS_1 to CS_4 which operate to provide non-interlace or of interlace operation.

For horizontal non-interlace there are two modes, the highest resolution and the half resolution mode, which provides a higher SNR. In the highest resolution mode, CS_1="1", CS_2="1", CS_3="0" and CS_4="0". With these control inputs, each amplifier selector $AS_{2p-1,2p}$ connects column lines Col_{2p-1} and Col_{2p} to inputs In_{2p-1} and In_{2p}, respectively, of sense amplifiers SA_{2p-1} and SA_{2p} and each column is read out separately.

For half resolution, CS_1="1", CS_2="0", CS_3="1" and CS_4="0". Amplifier selector $AS_{2p-1,2p}$ connects column lines Col_{2p-1} and Col_{i2p} to input In_{2p-1}. Inputs In_{2p} are not utilized and thus, sense

amplifiers SA_{2p} are not active. This configuration supports the modes depicted in Figs. 4B and 4C.

For horizontal interlace modes, odd columns are read out during the odd field readout and even columns are readout during the even field readout. In this mode, control signals CS_3="0" and CS_4="0" for the both fields. During the odd field readout, control signals CS_1="1" and CS_2="0", and only the odd columns Col_{2p-1} are read to the odd-indexed sense amplifiers SA_{2p-1}. Following the readout operation, the outputs of the odd-indexed sense amplifiers are multiplexed to video multiplexer 110. During the even field readout, control signals CS_1="0" and CS_2="1". This results in the even columns Col_{2p} being read to the even-indexed sense amplifiers SA_{2p}. Following the readout, the outputs of the even-indexed sense amplifiers SA_{2p} are multiplexed to the video multiplexer 110. Thus, in this mode of operation, image sensor 100 reads out the odd column pixels during the odd field and the even column pixels during the even field.

For the intercolumn and block interlace modes of Figs. 5B and 5C, column selector 108 operates as follows: for the odd field readout, control signals CS_1="1", CS_2="0", CS_3="1" and CS_4="0". Therefore, column lines Col_{2p-1} and Col_{2p} are connected to input In_{2p-1} of sense amplifiers SA_{2p-1}. Sense amplifiers SA_{2p} are disconnected. The charge from two column lines is steered and added together to a single odd-indexed sense amplifier SA_{2p-1}. For the even field readout, CS_1="0", CS_2="1", CS_3="0" and CS_4="1". Thus, column lines Col_{2p} and Col_{2p+1} are connected to the input In_{2p} of sense amplifier SA_{2p}. Sense amplifiers SA_{2p-1} are disconnected. For this field, the charge from two columns is steered and combined at a single even-indexed sense amplifier SA_{2p}.

Fig. 9 depicts the elements of video multiplexer 110, which comprises a sense amplifier unit 120, a column multiplexer 122 and a column decoder 124.

Sense amplifier unit 120 comprises sense amplifiers SA_i, one per column line Col_i.

Column decoder 124 controls which sense amplifier SA_i connects to a video output line V_x. Column decoder 124 outputs a single control output Cl_i at a time based on an input column address $(ColAdr_{L-1},ColAdr_{L-2},...,ColAdr_2,ColAdr_1,ColAdr_0)_2$ where $\log_2 N \leq L \leq \log_2 N-1$.

Thus, if

$$(38)\ i = \left(ColAdr_{L-1}, ColAdr_{L-2}, \ldots, ColAdr_2, ColAdr_1, ColAdr_0\right)_2 + 1$$

then Cl_i ="1", otherwise for $j \neq i$ Cl_j ="0"

Column multiplexer 122 connects the output of sense amplifier SA_i to video output line V_x. This is performed by activating a per-column transistor CT_i whose gate is connected to the per-column output Cl_i of column decoder 124.

Column selection is controlled thru the column address $ColAdr_0$-$ColAdr_{L-1}$ and the address sequence depends on the desired horizontal resolution.

For the highest resolution, non-interlace mode, the address is incremented by 1 each pixel cycle, starting with $(ColAdr_{L-1},ColAdr_{L-2},\ldots,ColAdr_2,ColAdr_1,ColAdr_0)_2$= 0 and ending with $(ColAdr_{L-1},ColAdr_{L-2},\ldots,ColAdr_2,ColAdr_1,ColAdr_0)_2$= N. For half the resolution, the address is incremented by 2 each pixel cycle.

The column address sequencing is identical for all interlace modes. During the odd field readout, the address is incremented by 2 each pixel cycle, starting with $(ColAdr_{L-1},ColAdr_{L-2},\ldots,ColAdr_2,ColAdr_1,ColAdr_0)_2$=0 and ending with $(ColAdr_{L-1},ColAdr_{L-2},\ldots,ColAdr_2,ColAdr_1,ColAdr_0)_2$= N. During the even field readout, the address is incremented by 2 each pixel cycle, starting with $(ColAdr_{L-1},ColAdr_{L-2},\ldots,ColAdr_2,ColAdr_1,ColAdr_0)_2$= 1 and ending with $(ColAdr_{L-1},ColAdr_{L-2},\ldots,ColAdr_2,ColAdr_1,ColAdr_0)_2$= N-1.

The image sensor of the present invention can be combined with the programmable resolution method of the invention described in US Serial Number 09/629,703, filed June 7, 1999, incorporated herein by reference, to accomplish a wider range of resolution/SNR combinations.

The methods and apparatus disclosed herein have been described without reference to specific hardware or software. Rather, the methods and apparatus have been described in a manner sufficient to enable persons of ordinary skill in the art to readily adapt commercially available

hardware and software as may be needed to reduce any of the embodiments of the present invention to practice without undue experimentation and using conventional techniques.

It will be appreciated by persons skilled in the art that the present invention is not limited by what has been particularly shown and described herein above. Rather the scope of the invention is defined by the claims that follow: